AMENDMENT TO THE CLAIMS

1-20. (Cancelled)

21. (New) A fabrication method of a memory device comprising:

a step of forming a memory cell with a capacitor including;

a sub-step of forming a first electrode on a substrate,

a sub-step of forming a ferroelectric film which is selectively grown on the first electrode, and

a sub-step of forming a second electrode on the ferroelectric film.

22. (New) The fabrication method of claim 21, wherein the ferroelectric film is made of a single crystal or a single domain.

23. (New) The fabrication method of claim 21, wherein a lattice constant of crystals of the first electrode is substantially the same as that of the ferroelectric film.

24. (New) The fabrication method of claim 21, wherein the ferroelectric film is grown to be self-organized by physical or chemical interaction between the ferroelectric film and the first electrode.

25. (New) The fabrication method of claim 24, wherein the ferroelectric film is grown in a vapor phase or in a liquid phase.

26. (New) The fabrication method of claim 24 further comprising:

a step of forming a selective switching device to be connected to the capacitor.

27. (New) The fabrication method of claim 26, wherein the selective switching device is formed on the substrate or between the substrate and the first electrode.

28. (New) The fabrication method of claim 26, wherein the selective switching device is a transistor or a bidirectional diode.

29. (New) A fabrication method of a memory device comprising:

a step of forming a first capacitor array layer including a plurality of capacitors; and

a step of forming a second capacitor array layer including a plurality of capacitors over the first capacitor array layer with an insulating film interposed between the first and the second capacitor array layers;

wherein the step of forming the first capacitor array layer includes;

a sub-step of forming a first electrode on a substrate,

a sub-step of forming a first ferroelectric film which is selectively grown on the first electrode, and

a sub-step of forming a second electrode on the first ferroelectric film; and

the step of forming the second capacitor array layer includes;

a sub-step of forming a third electrode on the substrate,

a sub-step of forming a second ferroelectric film which is selectively grown on the third electrode, and

a sub-step of forming a fourth electrode on the second ferroelectric film.

30. (New) The fabrication method of claim 29, wherein each of the first and the second ferroelectric films is made of a single crystal or a single domain.

31. (New) The fabrication method of claim 29, wherein a lattice constant of crystals of the first electrode is substantially the same as that of the first ferroelectric film and a lattice constant of crystals of the third electrode is substantially the same as that of the second ferroelectric film.

32. (New) The fabrication method of claim 29, wherein the first ferroelectric film is grown to be self-organized by physical or chemical interaction between the first ferroelectric film and the first electrode, and

the second ferroelectric film is grown to be self-organized by physical or chemical interaction between the second ferroelectric film and the third electrode.

33. (New) The fabrication method of claim 29, wherein each of the first and the second ferroelectric films is grown in a vapor phase or in a liquid phase.

34. (New) The fabrication method of claim 29 further comprising:

a step of forming selective switching devices to be respectively connected to the capacitors constituting the first and the second capacitor array layers, thereby forming respective memory cells.

35. (New) The fabrication method of claim 34, wherein each of the selective switching devices is formed on the substrate or between the substrate and the third electrode.

36. (New) The fabrication method of claim 34, wherein the selective switching devices are transistors or bidirectional diodes.

37. (New) The fabrication method of claim 34, wherein the selective switching devices respectively connected to the capacitors constituting the second capacitor array layer are formed in the second capacitor array layer.

38. (New) The fabrication method of claim 34, wherein the selective switching devices formed in the second capacitor array layer are thin film transistors or bidirectional diodes.

39. (New) The fabrication method of claim 34 further comprising:

a step of forming means for electrically connecting the memory cells included in the second capacitor array layer to one another between the first and the second capacitor array layers or on the second capacitor array layer.

40. (New) The fabrication method of claim 34 further comprising:

a step of forming means for electrically connecting the memory cells included in the first capacitor array layer to the memory cells included in the second capacitor array layer between the first and the second capacitor array layers.